AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

Claim 1. (currently amended) A bit-rate detection circuit for detecting a bit rate of a stream of input bits of SONET data having a pair of sequential framing bytes of value F6h and 28h, provided at a first, maximum rate, a second rate of half the maximum rate, or a third rate at a rate of a quarter of the maximum rate, comprising:

a plurality of shift registers adapted to serially shift in the input bits of SONET data having a data rate from a first transceiver, said shift registers being clocked at the first rate; and

logic circuitry responsively coupled to said shift registers and configured ~~adapted~~ to provide an output signal indicative of the data rate by

detecting a first pattern of 1010 or 0101 in first selected bits in the framing bytes in the shift registers,

detecting a second pattern of 101 or 010 in second selected bits in the framing bytes in the shift registers,

detecting a third pattern of 1001 or 0110 in third selected bits in the framing bytes in the shift registers, and

setting the value of the output signal to indicate the first, second or third rate in dependence upon which of the first, second and third patterns are detected.

Claim 2 (canceled)

Claim 3. (previously presented) The bit-rate detection circuit of Claim 1 wherein said logic circuitry is coupled to nodes between said shift registers.

Claim 4. (previously presented) The bit-rate detection circuit of Claim 3 wherein said logic circuitry comprises a first logic set, a second logic set and a third logic set each providing an output signal, said first logic set being coupled to a first set of said nodes between said shift registers and detecting the first pattern, and said second logic set being coupled to a second set of said nodes between said shift registers and detecting the second pattern, and said third logic set being coupled to a third set of said nodes between said shift registers and detecting the third pattern.

Claims 5 and 6 (canceled)

Claim 7. (previously presented) The bit-rate detection circuit of Claim 4, wherein said logic circuitry further comprises output logic circuitry responsively coupled to said first logic set, said second logic set and said third logic set, said output logic circuitry providing said output signal indicative of the data rate by providing the output signal:

indicating the first rate if said first logic set detects the first pattern,

indicating the second rate if said second logic set detects the second pattern and the first logic set does not detect the first pattern, and

indicating the third rate if said third logic set detects the third pattern, the first logic set does not detect the first pattern, and the second logic set does not detect the second pattern.

Claims 8-11 (canceled)

Claim 12. (previously presented) The bit-rate detection circuit of Claim 1 further comprising a communications transceiver module responsively coupled to said logic circuitry output signal and adapted to transmit data back to said first transceiver at said incoming data rate.

Claim 13. (previously presented) The bit-rate detection circuit of Claim 1 wherein said logic circuitry includes a single clock operating at the first rate.

Claims 14-30 (canceled)